# International Standard 6951

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# Information processing — Processor system bus interface (Eurobus A)

*Traitement de l'information — Bus d'interfaces entre processeurs (Eurobus A)*

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## Foreword

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Draft International Standards adopted by the technical committees are circulated to the member bodies for approval before their acceptance as International Standards by the ISO Council. They are approved in accordance with ISO procedures requiring at least 75 % approval by the member bodies voting.

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Users should note that all International Standards undergo revision from time to time and that any reference made herein to any other International Standard implies its latest edition, unless otherwise stated.



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# Contents

# Information processing — Processor system bus interface (Eurobus A)

## 0. Introduction

**0.1 General.** This standard specifies the set of signal lines that constitute the bus itself, and the interfacing of devices connected to the bus.

This standard specifies protocols for the allocation of bus time to devices wishing to make transfers and for the transfer of data between devices. The standard does not, however, specify priority rules, these being left to be formulated individually for each system.

This standard specifies a full set of signalling rules to be followed by the device responsible for bus allocation and by devices conducting transfers. Annex F gives illustrative examples of each of the possible types of transfer.

The set of electrical and signal timing requirements specified in clause 6 uniquely defines the interface that is Eurobus A. Certain mechanical requirements are specified in clause 6, namely those that directly affect the electrical characteristics (e.g. the physical length of the bus, the spacing of device connectors on the bus, the pin pitch on connectors and the signal disposition on the connectors), but this standard does not further specify the mechanical implementation. An example of a possible mechanical implementation of Eurobus A is given in annex J.

Implementations of Eurobus A are possible with 8, 16, 24, 32, . . . -bit data widths and devices having different data widths can operate on the same bus. Logical implementation summaries for the first four of the possible data widths are given in annexes A to D. Annex E specifies the connector allocation.

The group of signal lines constituting an assembled Eurobus A provides the means for the transfer of binary digital information between up to 20 devices plugged into the backplane of a single equipment shelf. Devices share the bus on a time-division multiplex basis. The length of the backplane is limited to a maximum of 460 mm. The signal lines form an asynchronous unbalanced voltage interface capable of operating at transfer rates of up to $6{,}5 \times 10^6$ words or bytes per second.

**0.2 Data width and addressing capability.** The data/address width of any device using the bus is theoretically unconstrained. However, the asynchronous protocols and addressing facilities of Eurobus A permit devices of 8, 16, 24 and 32-bit data widths to share the same bus, and when the bus is so shared, the maximum data width is that of the widest device.

The full addressing capability of the bus enables devices to address any 8-bit byte of any word in a normal address space defined by both of the following.

(a) The addressing range determined by the number of data/address bits.

(b) A two-bit extension to the foregoing (a). The full two-bit extension is available on buses with non-shared width, but on shared-width buses the use of these bits is restricted.

In addition, any complete word can be addressed in a second address space of equal magnitude to the first, designated the pseudo address space.

**0.3 Devices.** Free choice is available to the system designer as to the devices connected to a Eurobus and the order in which they are connected. However, each bus needs to include both:

(a) an arbiter, the purpose of which is to control the time-division multiplexing of transfers on the bus;

(b) if communication with other buses is required, a bus link to each of the other buses.

Figure 1 shows an example of a bus with a number of typical devices including an arbiter and a bus link.

**0.4 Bus allocation.** Information is transferred between devices on a master-and-slave basis. A device bids for control of the bus by means of its starred Request line and becomes the master device for that transfer after the arbiter has allocated the bus to it. This standard specifies the protocols by which devices bid for use of the bus and by which the arbiter allocates the use of the bus to one of them. The standard does not, however, specify the algorithm used in making the selection, thus the system designer is given the choice of an allocation algorithm in order to optimize system performance.

The protocol whereby a master device may flag an interrupt to the arbiter is also specified, but the subsequent action by the arbiter is left to the system designer to define.

**0.5 Bus transfers.** In addition to specifying the protocols for the execution of Read cycles (in which the master addresses a device as slave and reads data from it) and Write cycles (in which the master transfers data to the addressed slave), this standard also specifies the protocol for a Vector cycle in which an address, without data, is transferred from master to slave.

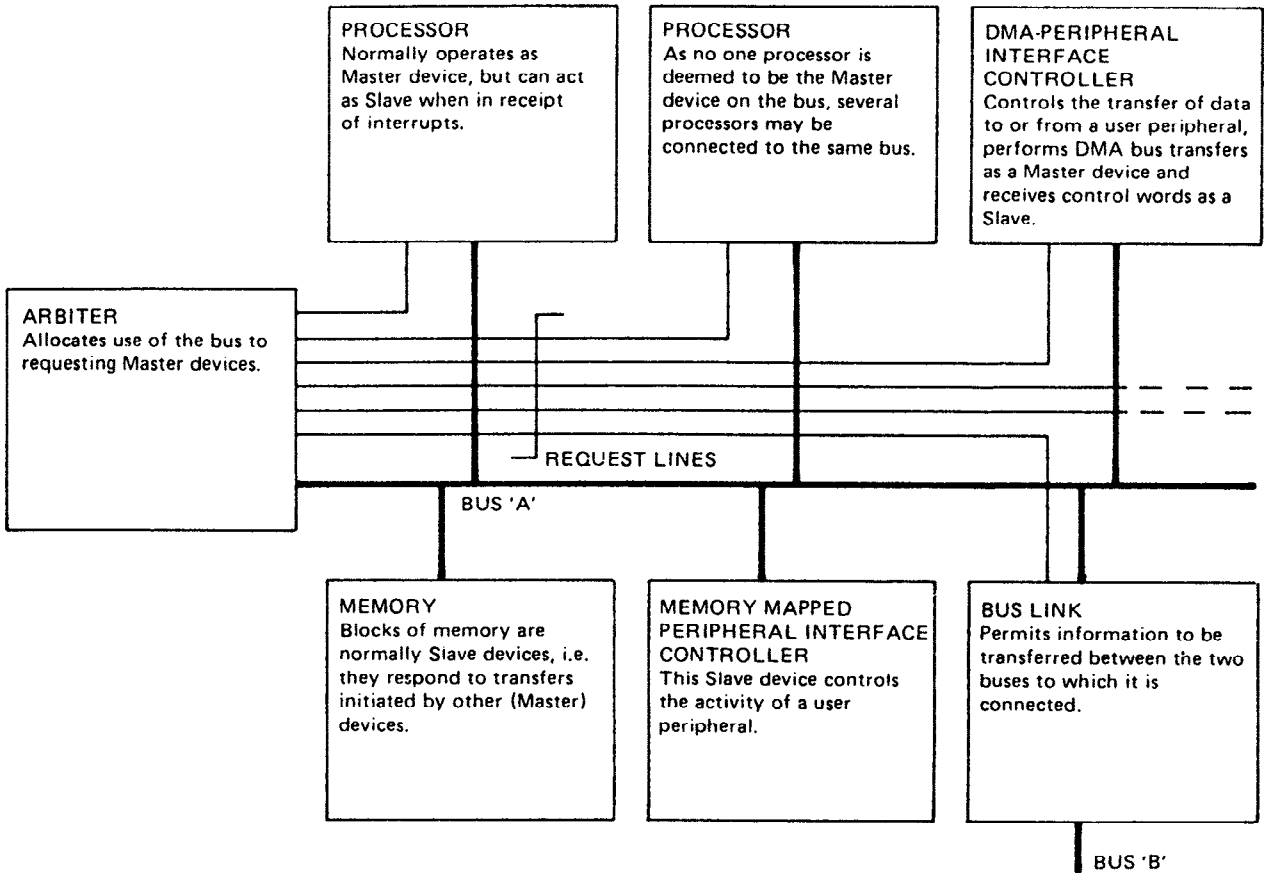


**Figure 1. Eurobus with some typical devices**

The bus allocation protocols permit a master to hold the bus for repeated use without the need to make a fresh bid for every transfer, while also giving the arbiter the ability to instruct any master to release the bus for reallocation. A master is also permitted to retain the bus for an indivisible sequence of cycles, such as a Read-Modify-Write sequence. An additional protocol is defined whereby the arbiter may abort a cycle that is deemed to have failed.

**0.6 Interbus transfers.** The protocols for Read, Write and Vector cycles permit a master on bus A, for example, wishing to effect a transfer with a slave on bus B, to address a bus linker on bus A as slave. The bus linker then bids for use of bus B as master and addresses the required slave on bus B. Should master devices on both buses attempt simultaneous transfers, the bus link cannot become master on either bus and a condition of deadly embrace ensues. The Eurobus protocols permit the embrace to be broken simply.

The protocols used by bus links to perform interbus addressing and data transfer are not within the scope of this standard.

**0.7 Electrical requirements.** The standard specifies the electrical and timing requirements that need to be obeyed by Eurobus A devices. Aspects covered within the electrical requirements include:

(a) the voltage levels of the active and quiescent logic states on the bus;

(b) the required characteristics of the termination networks;

(c) the required characteristics of the bus transmitters and receivers;

(d) the required characteristics of the spurs to be connected to the bus.

The specified set of electrical characteristics presupposes certain bus settling times for the transitions on the signal lines. Arising from these, certain timing constraints are specified. These constraints ensure that the relevant signal lines will have settled to the appropriate state before an associated control signal transition is issued.

**0.8 Commercial and military versions.** Two versions of Eurobus A are specified in this standard, a version for a commercial temperature range (0 °C to 70 °C) and a version for a military temperature range (−55 °C to 125 °C). Where the requirements are different they are separately specified for each version.

## 1. Scope and field of application

This International Standard specifies a processor system bus interface known as Eurobus A (referred to in the following text as "the bus") that is one of a family of interfaces for use in modular data acquisition, processing communication and control systems for military, industrial and other applications.

NOTE 1. More detailed information about the requirements specified in this International Standard, including the data width and addressing capability, devices connected to the bus, bus allocation, bus transfers, interbus transfers and electrical requirements, and background information are given in clause **0**.

NOTE 2. In this International Standard, upper case letters are used for the first letter of names of bus cycles.

NOTE 3. The titles of the publications referred to in this International Standard are listed in annex P.